REMARKS/ARGUMENTS

Claims 1-3, 5, 7-14, 16-21 and 23 remain in the application, all of which stand rejected.

1. Rejection of Claims 1-3, 5, 7-14, 16-21 and 23 Under 35 USC 103(a)

Claims 1-3, 5, 7-14, 16-21 and 23 stand rejected under 35 USC 103(a) as being unpatentable over Hisaka (US Pat. No. 5,334,889) in view of Williams et al. (US Pat. No. 3,798,471). For the details of his rejection, the Examiner refers applicants to the Office Action mailed 1/13/2005.

Given that applicants' claims have been amended since the Examiner's 1/13/2005 Office Action, applicants note that on 4/13/2005, claim 6 was incorporated into claim 1, and claim 24 was incorporated into claim 17. As a result, the Examiner's 1/13/2005 rejections of claims 6 and 24 now respectively apply to claims 1 and 17.

The Examiner asserts:

> As to claims 4, 6 and 24, note Fig. 1 of Hisaka, which shows a first switching circuit (the PFET within inverter 13), a first current clamp (R10), a delay circuit (inverters 14 and 15) and a FET (Tr15) is parallel with the resistor.

1/13/2005 Office Action, sec. 6, p. 6.

The teachings of Hisaka are duly noted. However, the Examiner fails to note that Hisaka's delay circuit 14, in combination with the inverter circuit 15, serves to bias FET Tr15 to an "off-state" at the time input signal S11 switches from a high level to a low level. As a result, Hisaka's FET Tr15 does not operate as a "non-persistent charge boost circuit" (like the FET recited in applicants' claim 1).

Applicants' above position is supported by Hisaka teachings at col. 3, lines 20-31, which state:

> As the level of the input signal S11, which is applied to the input electrode of the inverter circuit 13, shifts from a high to low level in the output buffer circuit

> of the above-described construction at a moment t0 as shown in (A) of FIG. 2, an output node n13 of the inverter circuit 13 rises from earth to the power source level as shown in (B) of FIG. 2. Since the fourth and fifth transistors Tr14, Tr15 are both in an off-state at this moment, the rising time of the node 13 takes an integrated form due to operation of the resistor R10 and the capacitor C10 and ***the voltage of the node n13 rises gradually as illustrated in (B) of FIG. 2.***

On the other hand, the driver circuit recited in applicants' claim 1 comprises "a first non-persistent charge boost circuit, ***to increase a rate at which the output of the driver circuit switches toward the first voltage***". Thus, Hisaka's FET Tr15 operates differently, and performs a different function, than the FET recited in applicants' claim 1.

Although the Examiner rejects claim 1 over the combined teachings of Hisaka and Williams, it seems to applicants that the Examiner's detailed rejection of claim 1 is supported by the teachings of Hisaka alone. However, and with respect to Williams' teachings, applicants do not believe that Williams discloses the "non-persistent charge boost circuit" driven by a "delay circuit" that is missing from Hisaka's teachings.

Applicants' claim 1 is believed to be allowable over Hisaka's and Williams' combined teachings for at least the above reasons. Claims 14 and 17 are believed to be allowable for similar reasons. Claims 2, 3, 5, 7-13, 16, 18-21 and 23 are believed to be allowable at least because they depend from one of claims 1, 14 or 17, or for reasons similar to why claim 1 is believed to be allowable.

2. Conclusion

In light of the amendments and remarks provided herein, applicants respectfully request the timely issuance of a Notice of Allowance.

Respectfully submitted,
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By: _____

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